ABSTRACT

A memory comprises at least one array of memory elements, a partition of the at least one array into a plurality of sub-arrays of the memory elements, and an array configuration circuit for selectively putting the at least one array in one of two operating configurations. In a first operating configuration, the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, while in a second operating configuration the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block, a data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array. A sub-array selector, responsive to a first memory address, selects one among the at least two sub-arrays according to the first memory address, and enables access to the selected sub-array. A memory element access circuit, responsive to a second memory address, enables access to a prescribed memory element in the selected sub-array after a prescribed number of shifts of the data content of the memory elements in the selected sub-array depending on the second memory address.